EZ-PD™ CCG2 USB Type-C port controller

General description

EZ-PD™ CCG2 is a USB Type-C controller that complies with the latest USB Type-C and Power Delivery (PD) standards. EZ-PD™ CCG2 provides a complete USB Type-C and USB PD port control solution for passive cables, active cables, and powered accessories. It can also be used in many upstream and downstream facing port applications. EZ-PD™ CCG2 uses Infineon's proprietary M0 technology with a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 32-KB flash and integrates a complete Type-C transceiver including the Type-C termination resistors R_P, R_D, and R_A.

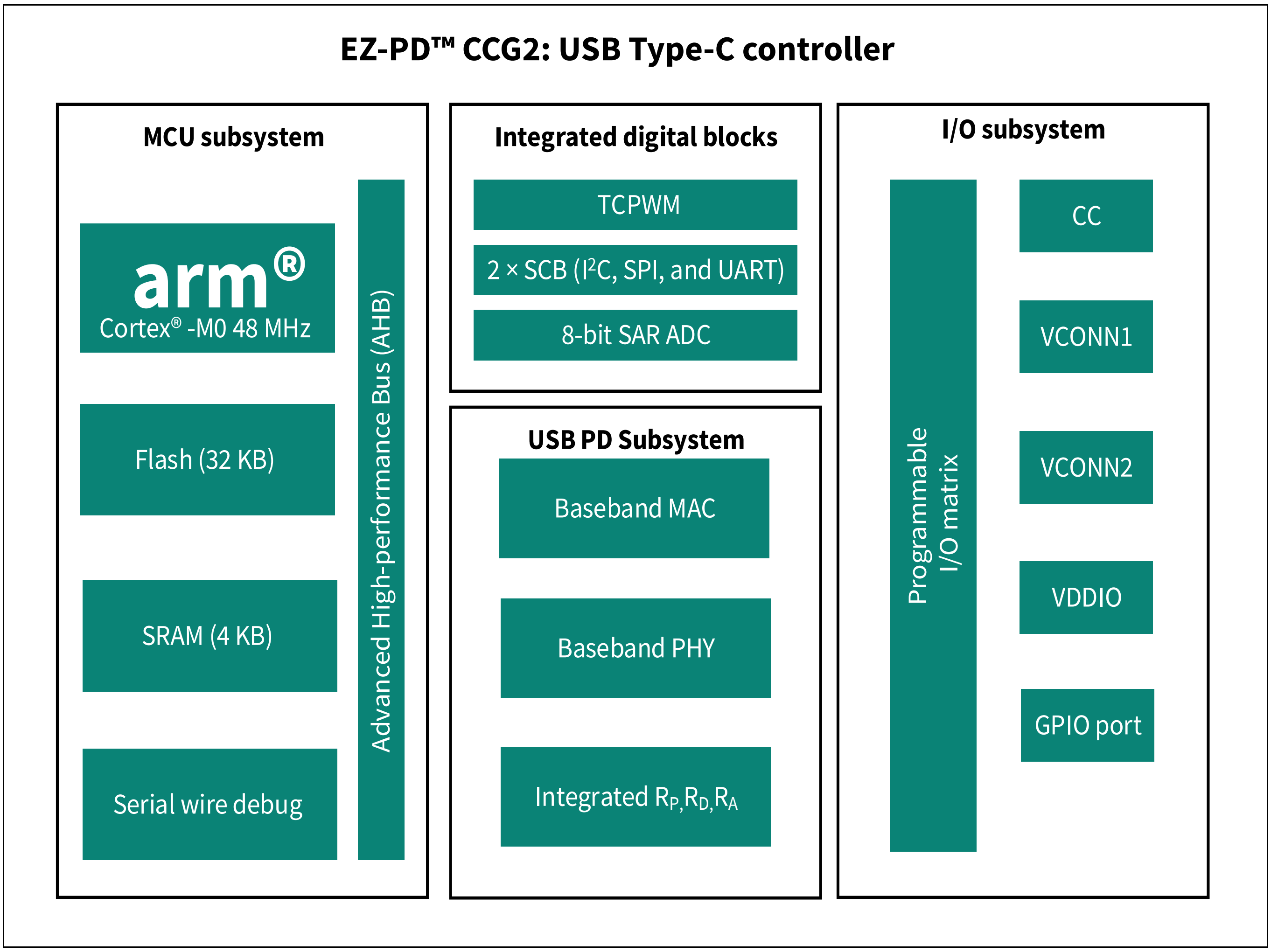
Applications

- USB Type-C EMCA cables
- USB Type-C powered accessories
- USB Type-C upstream facing ports
- USB Type-C downstream facing ports

Features

- 32-bit MCU subsystem
  - 48-MHz Arm® Cortex®-M0 CPU
  - 32-KB flash
  - 4-KB SRAM
  - In-system reprogrammable
- Integrated digital blocks
  - Integrated timers and counters to meet response times required by the USB-PD protocol
  - Run-time reconfigurable serial communication block (SCB) with reconfigurable I^2C, SPI, or UART functionality
- Clocks and oscillators
  - Integrated oscillator eliminating the need for external clock
- Type-C support
  - Integrated transceiver (baseband PHY)
  - Integrated UFP (R_D), EMCA (R_A) termination resistors, and current sources for DFP (R_P)
  - Supports one USB Type-C port
- Low-power operation
  - 2.7 V to 5.5 V operation
  - Two independent VCONN rails with integrated isolation between the two
  - Independent supply voltage pin for GPIO that allows 1.71-V to 5.5-V signaling on the I/Os
  - Reset: 1.0 µA, Deep Sleep: 2.5 µA, Sleep: 2.0 mA
- System-level ESD on CC and VCONN pins
  - ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C
- Packages
  - 1.63 mm × 2.03mm × 20-ball wafer-level CSP (WLCSP) with 0.4-mm ball pitch
  - 4.0 mm × 4.0 mm, 0.55 mm 24L QFN
  - Supports industrial (-40°C to +85°C) and extended industrial (-40°C to +105°C) temperature ranges

Logic block diagram



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1 Available firmware and software tools

1.1 EZ-PD™ Configuration Utility

The EZ-PD™ Configuration Utility is a GUI-based Microsoft® Windows application developed by Infineon to guide a CCGx user through the process of configuring and programming the chip. The utility allows users to:

- Select and configure the parameters they want to modify
- Program the resulting configuration onto the target CCGx device

The utility works with the Infineon supplied CCG1, CCG2, CCG3, and CCG4 kits, which host the CCGx controllers along with a USB interface. This version of the EZ-PD™ Configuration Utility supports configuration and firmware update operations on CCGx controllers implementing EMCA and display dongle applications. Support for other applications, such as power adapters and notebook port controllers, will be provided in later versions of the utility.

For the application and its associated documentation, see the **USB EZ-PD™ Configuration Utility** web page.

2 EZ-PD™ CCG2 block diagram

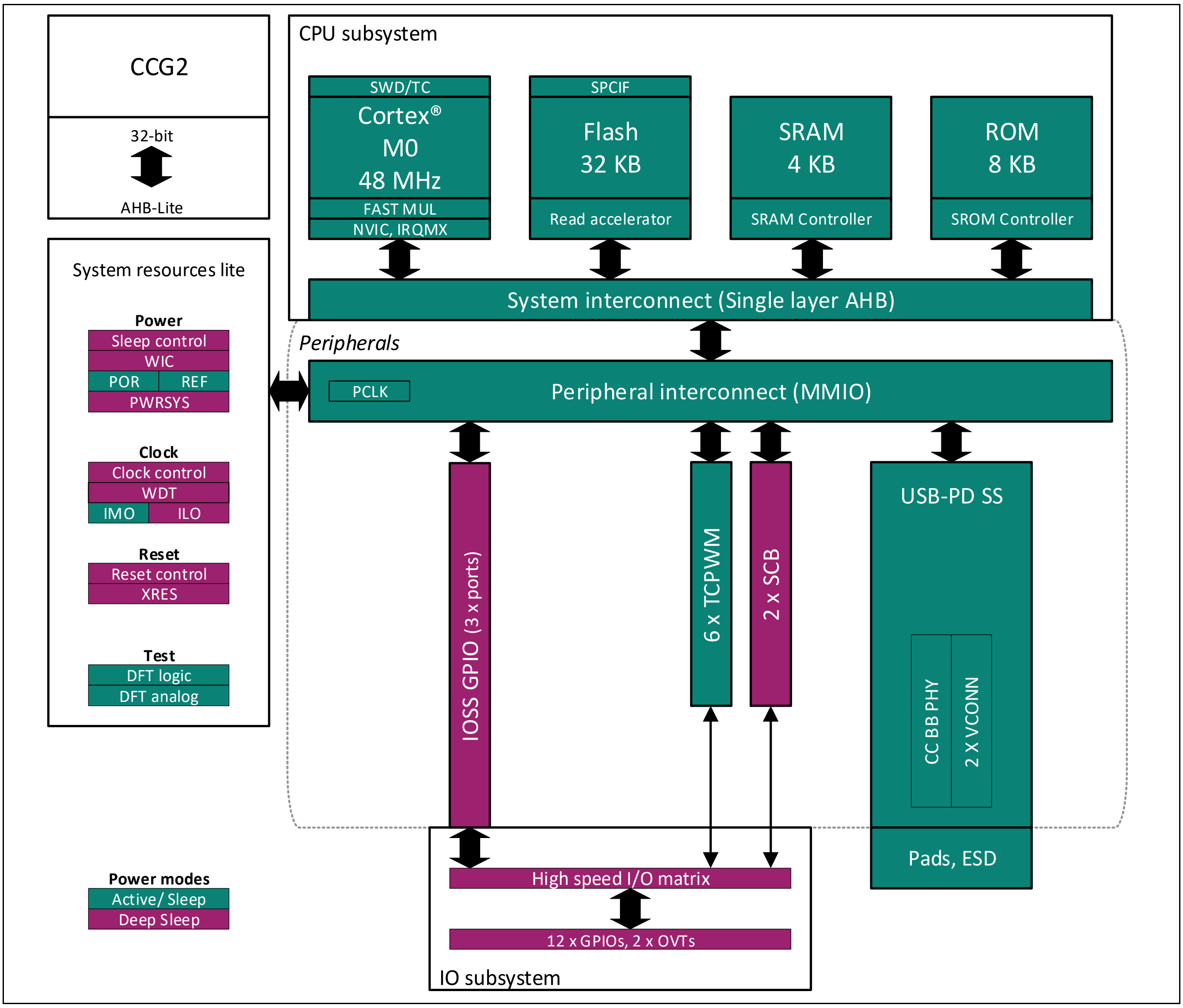


Figure 1 **EZ-PD™ CCG2 block diagram**

3 Functional overview

3.1 CPU and memory subsystem

3.1.1 CPU

The Cortex®-M0 CPU in EZ-PD™ CCG2 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex®-M3 and M4, thus enabling upward compatibility. The Infineon implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor up from the Deep Sleep mode, allowing power to be switched off to the main processor when the chip is in the Deep Sleep mode. The Cortex®-M0 CPU provides a non-maskable interrupt (NMI) input, which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD™ CCG2 has four break-point (address) comparators and two watchpoint (data) comparators.

3.1.2 Flash

The EZ-PD™ CCG2 device has a flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 1 wait-state (WS) access time at 48 MHz and with 0-WS access time at 24 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

3.1.3 SROM

A supervisory ROM that contains boot and configuration routines is provided.

3.2 USB-PD subsystem (SS)

EZ-PD™ CCG2 has a USB-PD subsystem consisting of a USB Type-C baseband transceiver and physical-layer logic. This transceiver performs the BMC and the 4b/5b encoding and decoding functions as well as the 1.2-V front end. This subsystem integrates the required termination resistors to identify the role of the EZ-PD™ CCG2 solution. R_A is used to identify EZ-PD™ CCG2 as an accessory or an electronically marked cable. R_D is used to identify EZ-PD™ CCG2 as a UFP in a hybrid cable or a dongle. When configured as a DFP, integrated current sources perform the role of R_P or pull-up resistors. These current sources can be programmed to indicate the complete range of current capacity on VBUS defined in the Type-C spec. EZ-PD™ CCG2 responds to all USB-PD communication. The EZ-PD™ CCG2 USB-PD subsystem can be configured to respond to SOP, SOP', or SOP” messaging.

The USB-PD subsystem contains a 8-bit successive approximation register (SAR) ADC for analog to digital conversions. The ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex buses an internal bandgap voltage and an internal voltage proportional to the absolute temperature. All GPIO inputs can be connected to the global analog multiplex buses through a switch at each GPIO that can enable that GPIO to be connected to the MUX bus for ADC use. The CC1, CC2, and RD1 pins are not available to connect to the MUX buses.

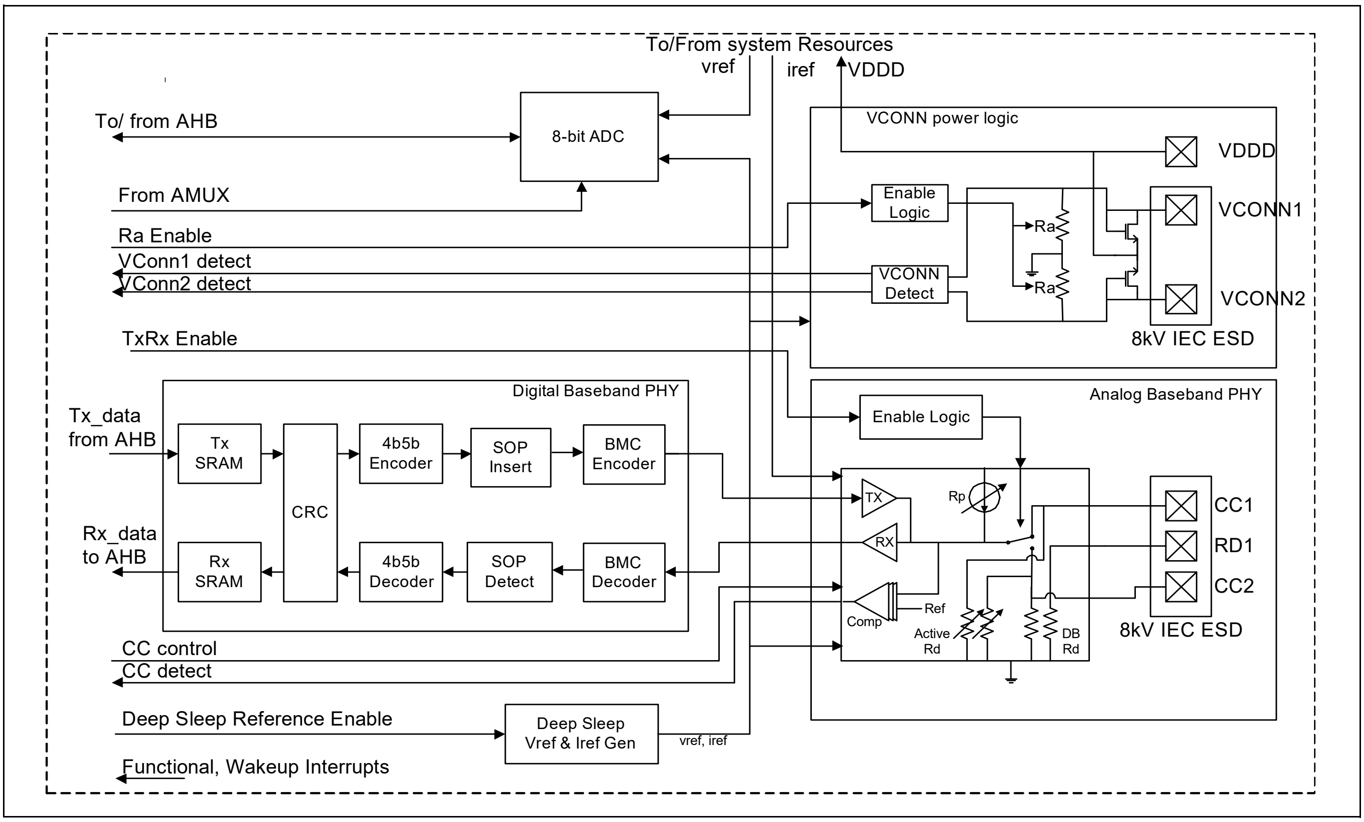


Figure 2 **USB-PD subsystem**

3.3 System resources

3.3.1 Power system

The power system is described in detail in the section **Power on page 12**. It provides the assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low voltage detect (LVD)). EZ-PD™ CCG2 can operate from three different power sources over the range of 2.7 V to 5.5 V and has three different power modes, transitions between which are managed by the power system. EZ-PD™ CCG2 provides Sleep and Deep Sleep low-power modes.

3.3.2 Clock system

The clock system for EZ-PD™ CCG2 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO).

3.4 Peripherals

3.4.1 Serial communication blocks (SCB)

EZ-PD™ CCG2 has two SCBs, which can be configured to implement an I^2C, SPI, or UART interface. The hardware I^2C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I^2C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I^2C that creates a mailbox address range in the memory of EZ-PD™ CCG2 and effectively reduce I^2C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read data on time.

The I^2C peripherals are compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (**UM10204**). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

The I^2C port on SCB 1 block of EZ-PD™ CCG2 is not completely compliant with the I^2C spec in the following:

- The GPIO cells for SCB 1's I^2C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I^2C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

3.4.2 Timer/counter/PWM block (TCPWM)

EZ-PD™ CCG2 has six TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

3.5 GPIO

EZ-PD™ CCG2 has up to ten GPIOs in addition to the I^2C and SWD pins, which can also be used as GPIOs. The I^2C pins from SCB 0 are overvoltage-tolerant. The number of available GPIOs vary with the package. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, the I/O pins are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

4 Pinouts

Table 1 Pinouts

Group	Name	Pin map 24L QFN	20-ball location	Description
USB Type-C port	CC1	2	B4	USB PD connector detect/configuration channel 1
	CC2	1	A4	USB PD connector detect/configuration channel 2
	RD1	3	B3	Dedicated R_d resistor pin for CC1. Must be left open for cable applications and connected together with CC1 ball for UFP or DFP with dead battery applications.
GPIOs and serial interfaces	GPIO	22	C3	GPIO / SPI_0_CLK / UART_0_ RX
	GPIO	18	D3	GPIO / SPI_0_MOSI / UART_0_TX
	GPIO	13	C2	GPIO / I2C_1_SDA / SPI_1_MISO / UART_1_RX
	GPIO	10	D2	GPIO / I2C_1_SCL / SPI_1_CLK / UART_1_TX
	GPIO	15	B2	GPIO / SPI_1_SEL / UART_1_RTS
	GPIO	14	N/A	
	GPIO	17	N/A	
	GPIO	21	N/A	GPIO
	GPIO	23	N/A	
	GPIO	24	N/A	
	I2C_0_SCL	20	A3	GPIO / I2C_0_SCL / SPI_0_MISO / UART_0_RTS
	I2C_0_SDA	19	A2	GPIO / I2C_0_SDA / SPI_0_SEL / UART_0_CTS
	SWD _IO	11	E2	SWD IO / GPIO / UART_1_CTS / SPI_1_MOSI
	SWD_CLK	12	D1	SWD clock / GPIO
Reset	XRES	16	B1	Reset input
Power	VCONN1	5	E4	VCONN 1 input (4.0 V to 5.5 V)
	VCONN2	4	C4	VCONN 2 input (4.0 V to 5.5 V)
	VDDIO	8	E1	1.71-V to 5.5-V supply for I/Os
	VCCD	7	A1	1.8-V regulator output for filter capacitor
	VDDD	9	E3	VDDD supply input/output (2.7 V to 5.5 h V)
	VDDD	6		
	VSS		N/A	
	VSS	EPAD	D4	Ground supply
	VSS		C1	

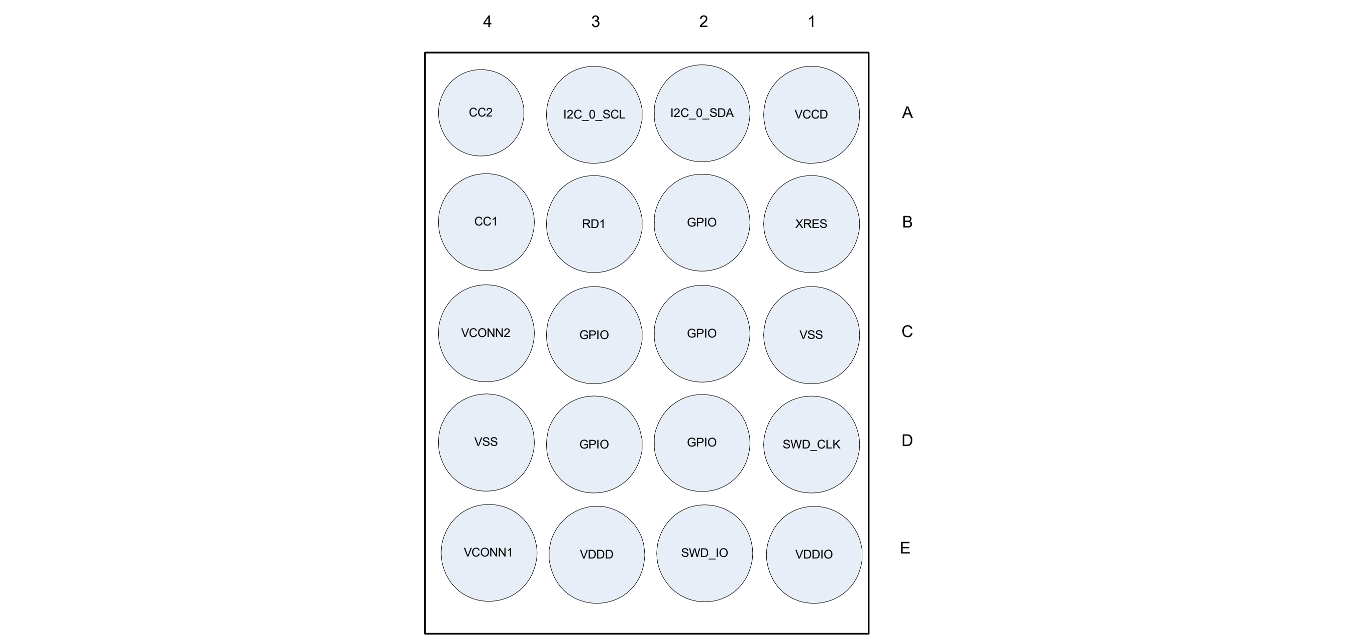


Figure 3 **20-ball WLCSP EZ-PD™ CCG2 ball map (bottom view)**

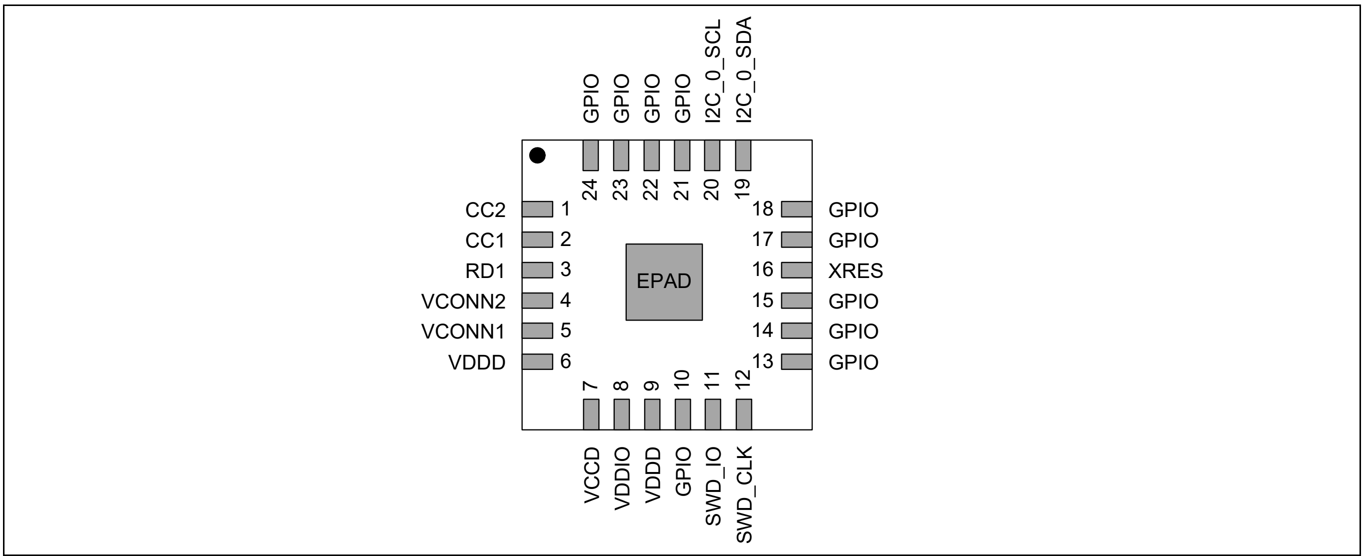


Figure 4 **24L QFN pin map (top view)**

5 Power

The following power system diagram shows the set of power supply pins as implemented in EZ-PD™ CCG2.

EZ-PD™ CCG2 can operate from three different power sources. VCONN1 and VCONN2 pins can be used as connections to the VCONN pins on a Type-C plug of a cable or VCONN-powered accessory. Each of these inputs support operation over 4.0 V to 5.5 V. An internal isolation between VCONN1 and VCONN2 pins is provided allowing them to be at different levels simultaneously. CCG2 can be used in EMCA applications with only one or both VCONN pins as power sources. This is illustrated later in the section on applications. Besides being power inputs, each VCONN pin is also internally connected to a R_A termination resistor required for EMCA and VCONN-powered accessories.

EZ-PD™ CCG2 can also be operate from 2.7 V to 5.5 V when operated from the VDDD supply pin. VCONN-powered accessory applications require that CCG2 work down to 2.7 V. In such applications, both the VDDD and VCONN pins should be connected to the VCONN pin of the Type-C plug in the accessory.

In UFP, DFP, and DRP applications, CCG2 can be operated from VDDD as the only supply input. In such applications, the VCONN pins are left open. In DFP applications, the lowest VDDD level that CCG2 can operate is 3.0 V due to the need to support disconnect detection thresholds of up to 2.7 V.

A separate I/O supply pin, VDDIO, allows the GPIOs to operate at levels from 1.71 V to 5.5 V. The VDDIO pin can be equal to or less than the voltages connected to the VCONN1, VCONN2, and VDDD pins.

The VCCD output of EZ-PD™ CCG2 must be bypassed to ground via an external capacitor (in the range of 1 to 1.6 µF; X5R ceramic or better).

Bypass capacitors must be used from VDDD and VCONN pins to ground; typical practice for systems in this frequency range is to use a 0.1-µF capacitor. Note that these are simply rules of thumb and that for critical applications, the PCB layout, lead inductance, and the bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 5 shows an example of the power supply bypass capacitors.

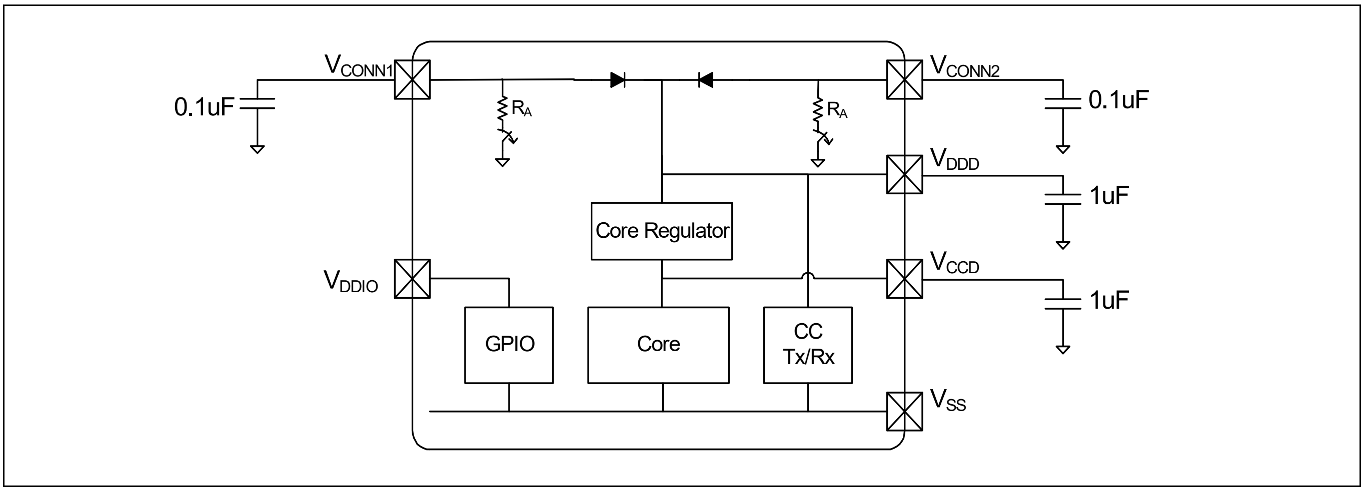


Figure 5 **EZ-PD™ CCG2 power and bypass scheme example**

6 CCG2 programming and bootloading

There are two ways to program application firmware into a CCG2 device:

1. Programming the device flash over SWD Interface
2. Application firmware update over specific interfaces (CC, I^2C)

Generally, the CCG2 devices are programmed over SWD interface only during development or during the manufacturing process of the end product. Once the end product is manufactured, the CCG2 device's application firmware can be updated via the appropriate bootloader interface. However, it is recommended to disable the update over bootloader interface before the end product goes to mass production, unless a secure method of firmware update is implemented by the customer.

6.1 Programming the CCG2 device flash over SWD interface

The CCG2 family of devices can be programmed using the SWD interface. Infineon provides programming kits (**CY8CKIT-002 MiniProg3 Kit**) called MiniProg3 and (**CY8CKIT-005 MiniProg4 Kit**) MiniProg4 which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in **PSoC Creator Software**. Click **here** for more information on how to use the MiniProg3 programmer. Click **here** for more information on how to use the MiniProg4 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in **Figure 6**, the SWD_IO and SWD_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, the device can be powered by the host programmer by connecting its VTARG (power supply to the target device) to VDDD pin of CCG2 device. If the CCG2 device is powered using an on-board power supply, it can be programmed using the "Reset Programming" option. For more details, contact **Infineon support** for CCGx programming specifications.

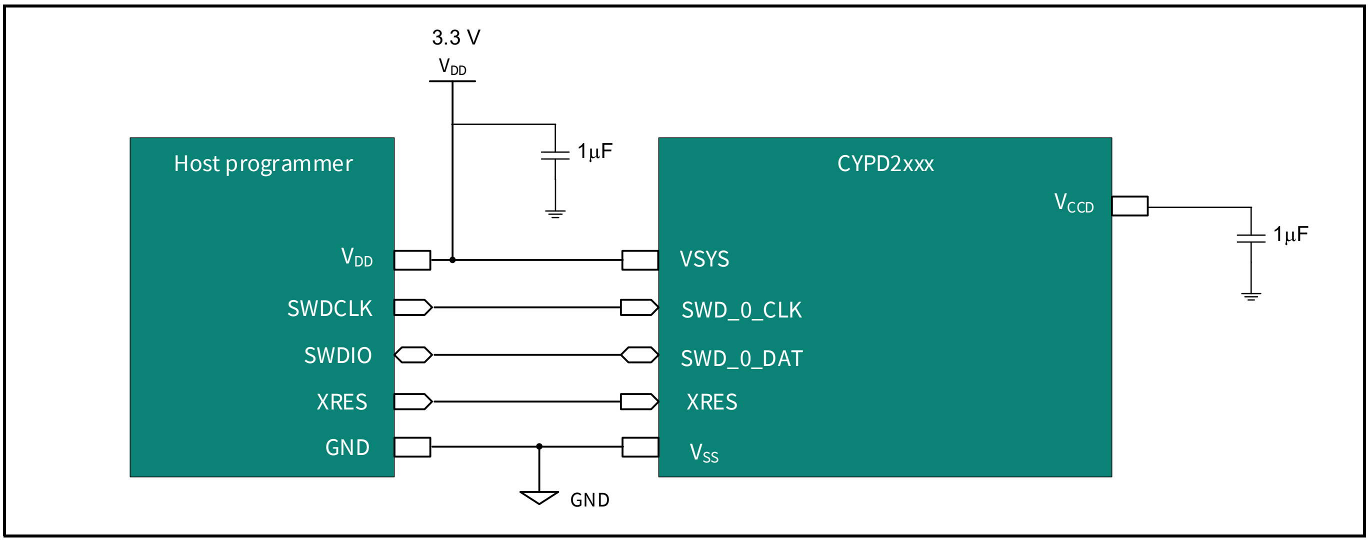


Figure 6 Connecting the programmer to CCG2 device

6.2 Application firmware update (I^2C, CC)

The application firmware can be updated over two different interfaces depending on the default firmware programmed into the CCG2 device. Refer to **Table 28** for more details on default firmware that various part numbers of the CCG2 family of devices are preprogrammed with (note that some of the devices have bootloader only and some have bootloader plus application firmware).

6.2.1 Application firmware update over I^2C interface

This method primarily applies to CYPD2104 and CYPD2122 devices of the CCG2 family. In these applications, the CCG2 device interfaces to an on-board application processor or an embedded controller or a billboard device that will act as a USB to I^2C bridge over I^2C interface. Refer to **Figure 7** for more details.

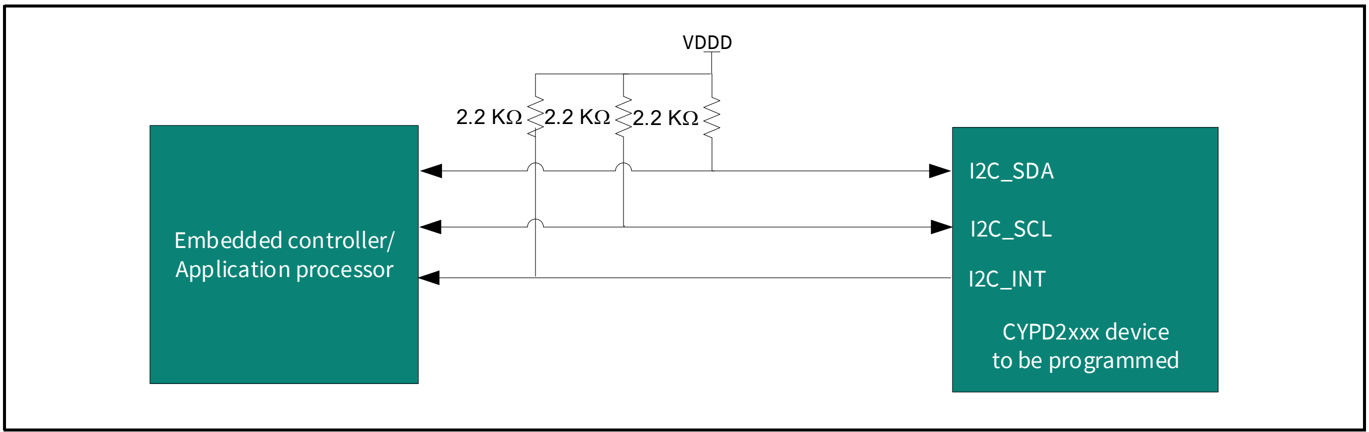


Figure 7 Application firmware update over I^2C interface

6.2.2 Application firmware update over CC interface for DFP applications

This method primarily applies to the CYPD2134 device of the CCG2 family. For bootloading, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Infineon-specific Vendor Defined Messages (VDMs) over the CC line. The CY4532 EVK's base board is connected to the system containing CCG2 device on one end and a Windows PC running the **EZ-PD™ Configuration Utility** as shown in **Figure 8** on the other end to bootload the CCG2 device.

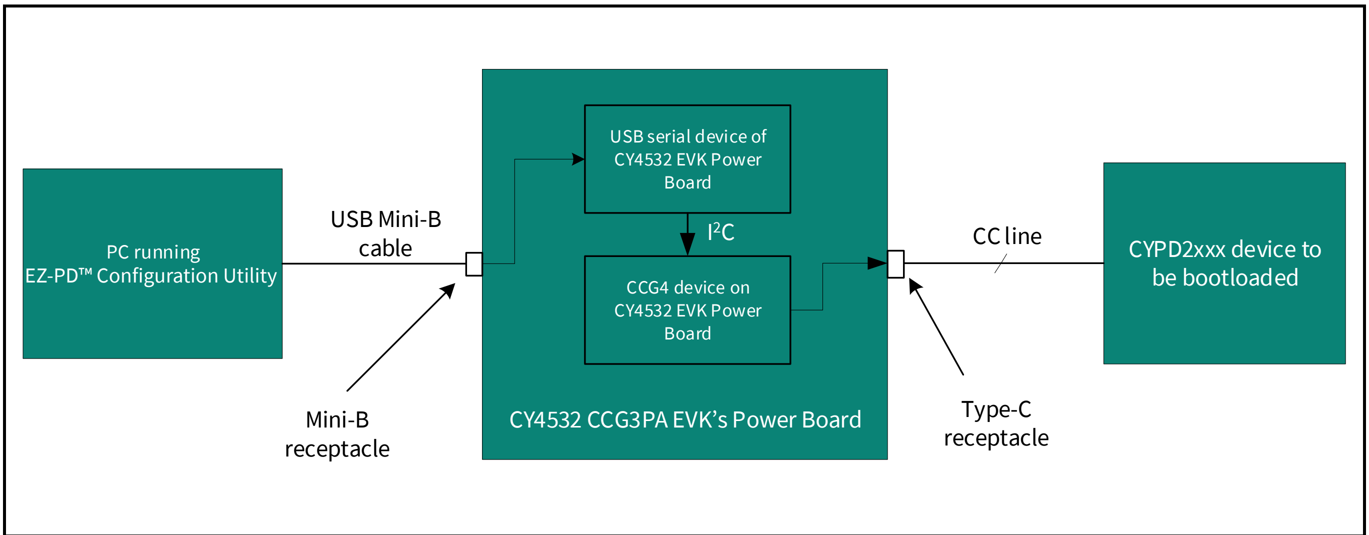


Figure 8 Application firmware update over CC interface for DFP applications

6.2.3 Application firmware update over CC interface for cable applications

This method primarily applies to the CYPD2105 devices of the CCG2 family. Refer to the **EZ-PD™ Configuration Utility user manual** for further details on how to do the application firmware update over CC interface for cable applications.

7 Application diagrams

7.1 EMCA Applications

Figure 9 to **Figure 12** show the application diagrams of a Passive EMCA application using CCG2 devices. **Figure 9** and **Figure 10** show the application using a single CCG2 device per cable present at one of the two plugs, whereas **Figure 11** and **Figure 12** show the same with two CCG2 devices per cable present at each plug. The VBUS signal, the SuperSpeed lines, HighSpeed lines, and CC lines are connected directly from one end to another.

The application diagrams shown in **Figure 9** and **Figure 10** require a single VCONN wire to run through the cable so that the CCG2 device can be powered irrespective of which plug is connected to the host (DFP). However, in the application diagrams shown in **Figure 11** and **Figure 12**, the VCONN signal does not run through the entire cable, but only runs to the respective VCONN pin of the CCG2 device at each end of the plug. Also, only one CCG2 device is powered at any given instance, depending on which one is nearer to the DFP that supplies VCONN.

Note: Application diagram in **Figure 10** requires external diodes to operate in the extended VCONN voltage range of 2.7 V to 5.5 V.

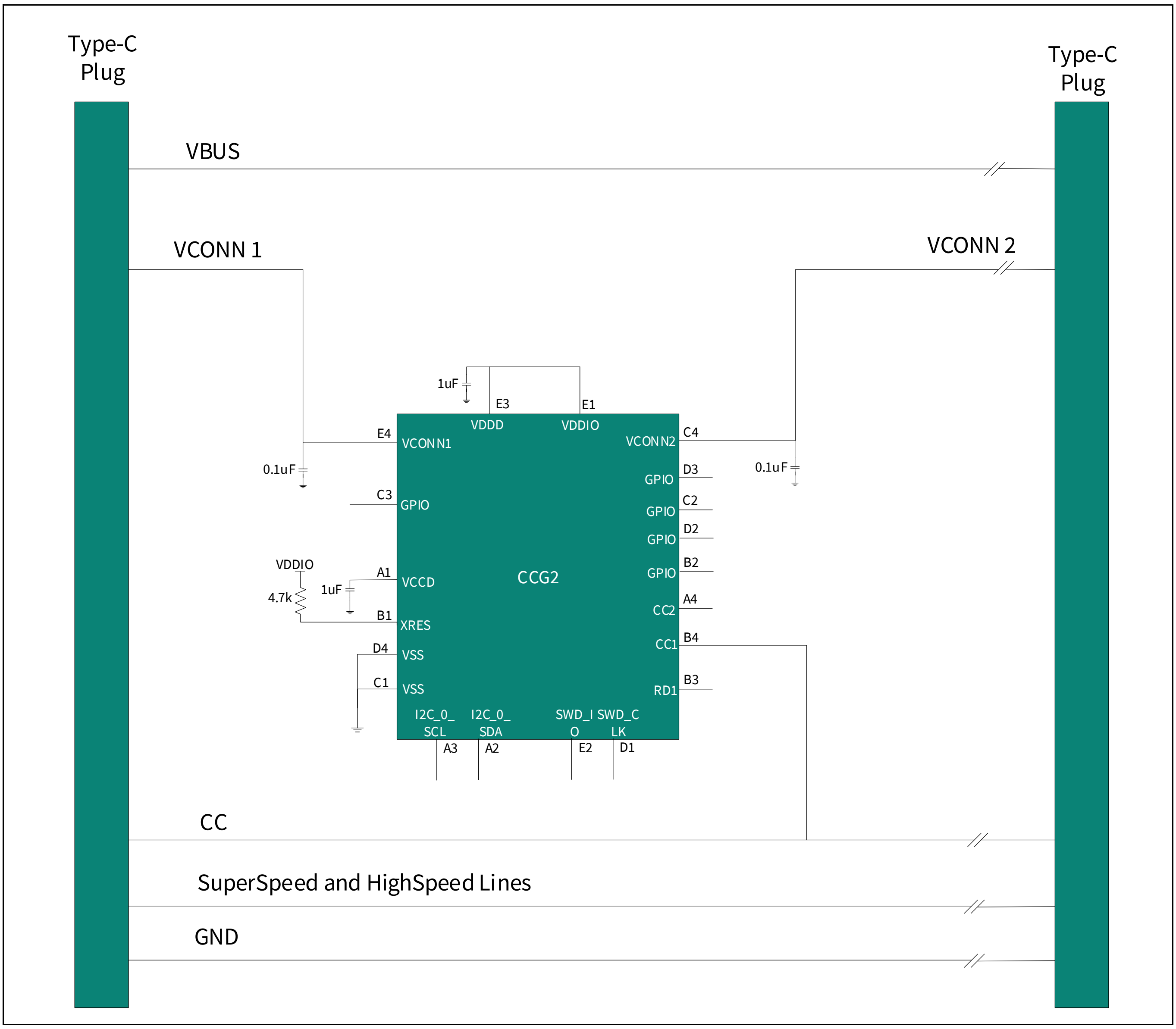


Figure 9 **Passive EMCA application – Single EZ-PD™ CCG2 per cable (VCONN range between 4.0 V to 5.5 V)**

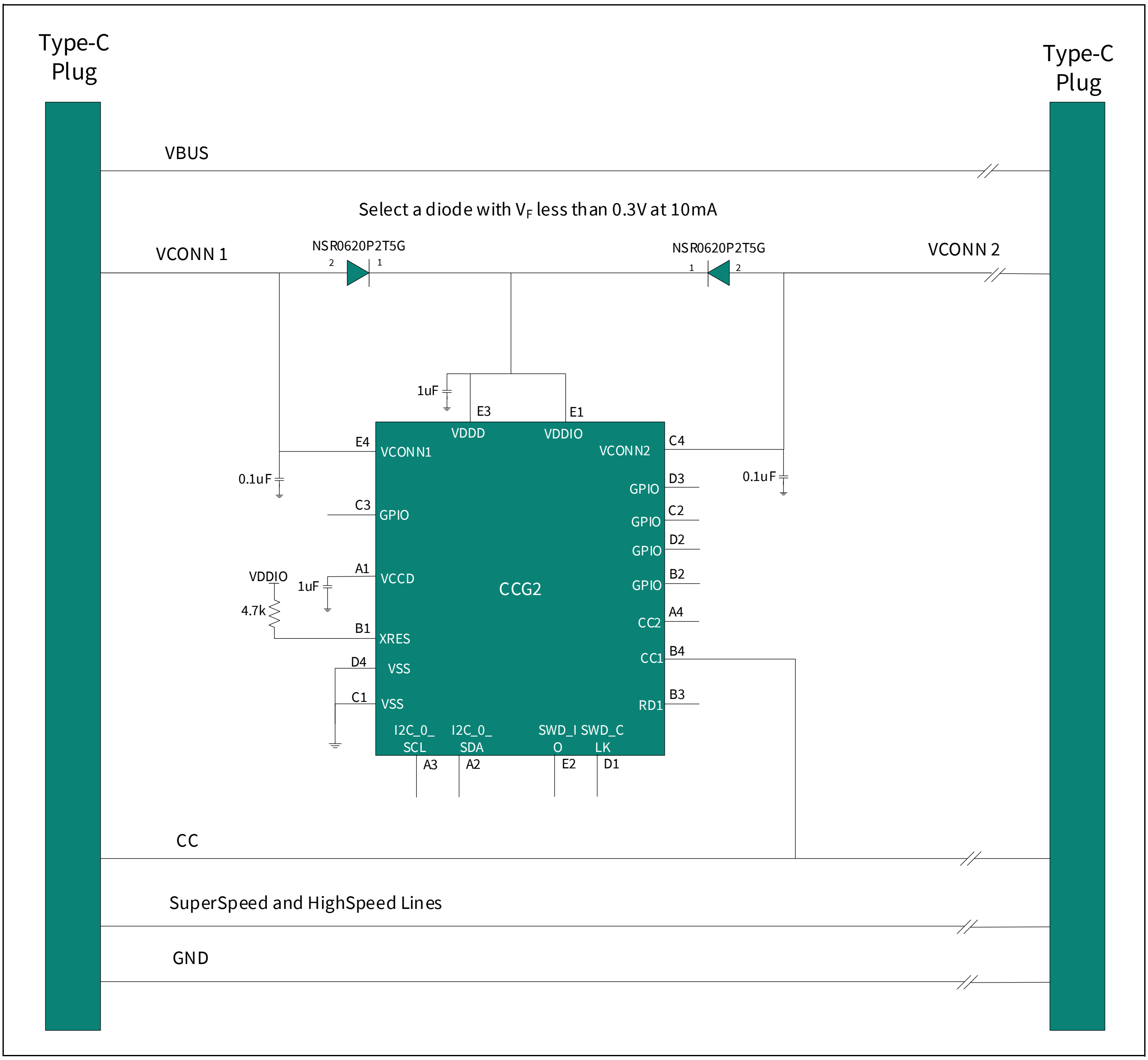


Figure 10 **Passive EMCA application – Single EZ-PD™ CCG2 per cable (VCONN range between 2.7 V to 5.5 V)**

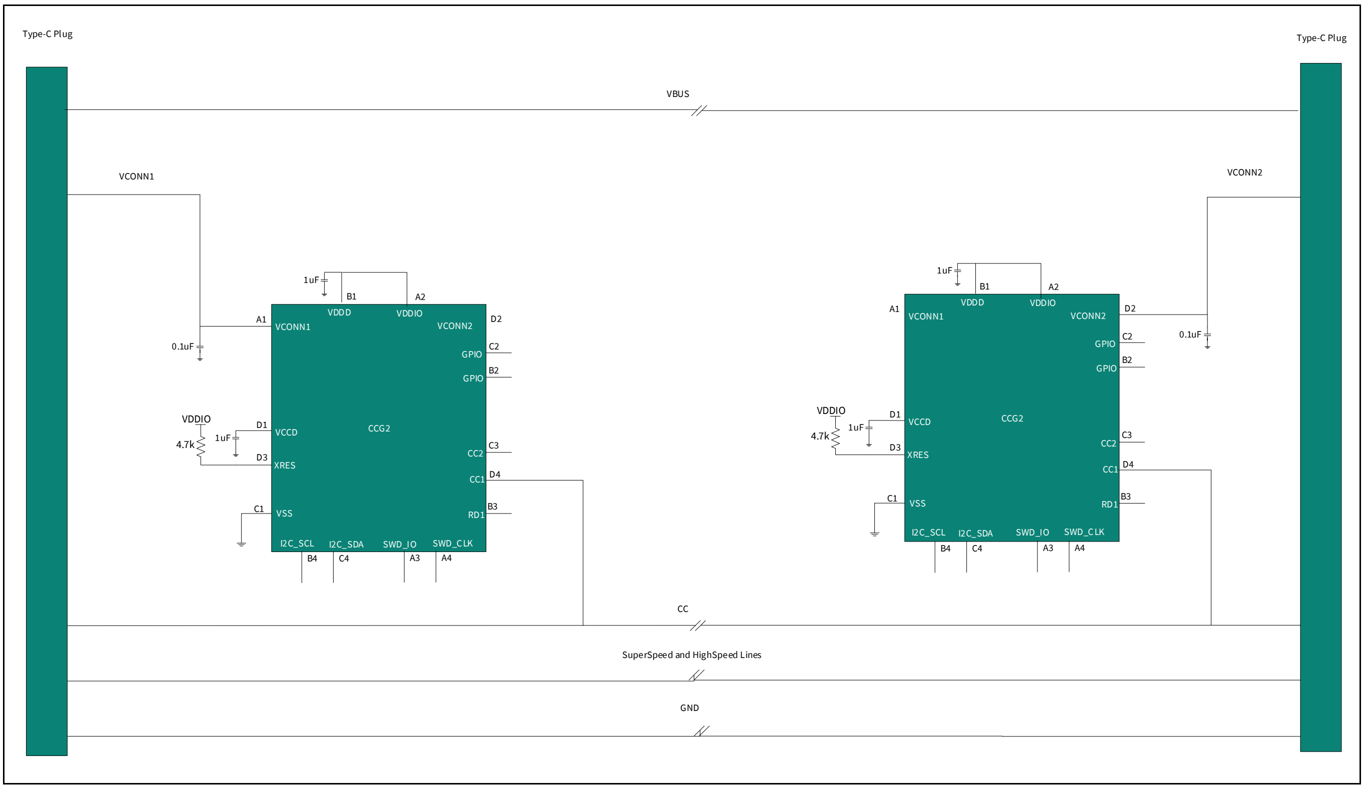


Figure 11 **Passive EMCA application (PD3.0/USB4) – Single EZ-PD™ CCG2 per plug (VCONN range between 4.0 V to 5.5 V)**

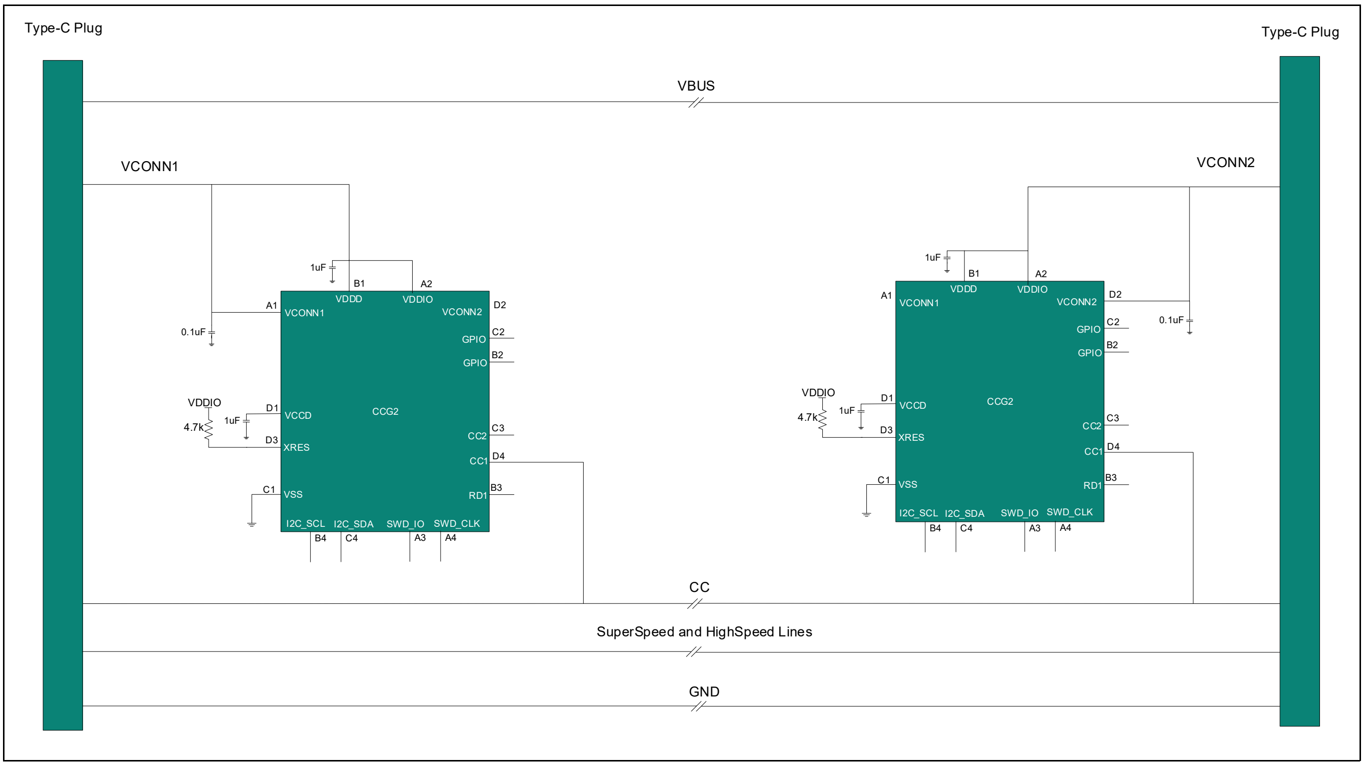


Figure 12 **Passive EMCA application – Single EZ-PD™ CCG2 per plug (VCONN range between 2.7 V to 5.5 V)**

7.2 Upstream facing port applications

Figure 13 shows a CCG2 device being used in a UFP application (tablet with a Type-C port) only as a power consumer.

The Type-C receptacle brings in HighSpeed and SuperSpeed lines, which are connected directly to the applications processor. The VBUS line from the Type-C receptacle goes directly to the UFP (tablet) charger circuitry. The applications processor communicates over the I^2C signal with the CCG2 device, and the CC1 and CC2 lines from the Type-C receptacle are connected directly to the respective CC1/2 pins of the CCG2 device.

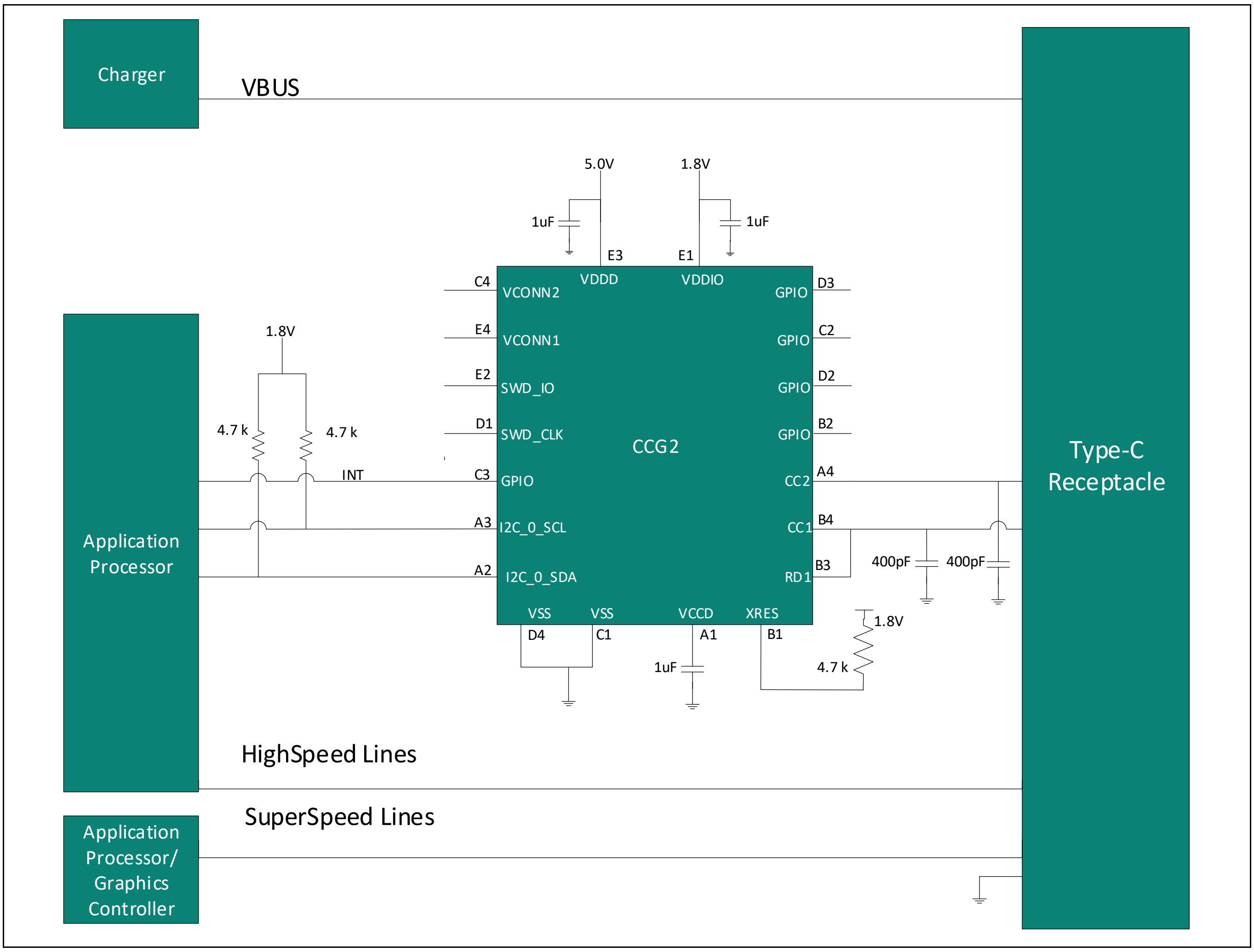


Figure 13 Upstream facing port (UFP) application – Tablet with a Type-C port

7.3 Notebook applications

Figure 14 shows a Notebook DRP application diagram using a CCG2 device. The Type-C port can be used as a power provider or a power consumer. The CCG2 device communicates with the embedded controller (EC) over I^2C. It also controls the Data MUX to route the High Speed signals either to the USB chipset (during Normal mode) or the DisplayPort Chipset (during Alternate mode). The SBU lines, SuperSpeed and HighSpeed lines are routed directly from the Display MUX of the notebook to the Type-C receptacle.

Optional FETs are provided for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. A VBUS_DISCHARGE FET controlled by CCG2 device is used to quickly discharge VBUS after the Type-C connection is detached.

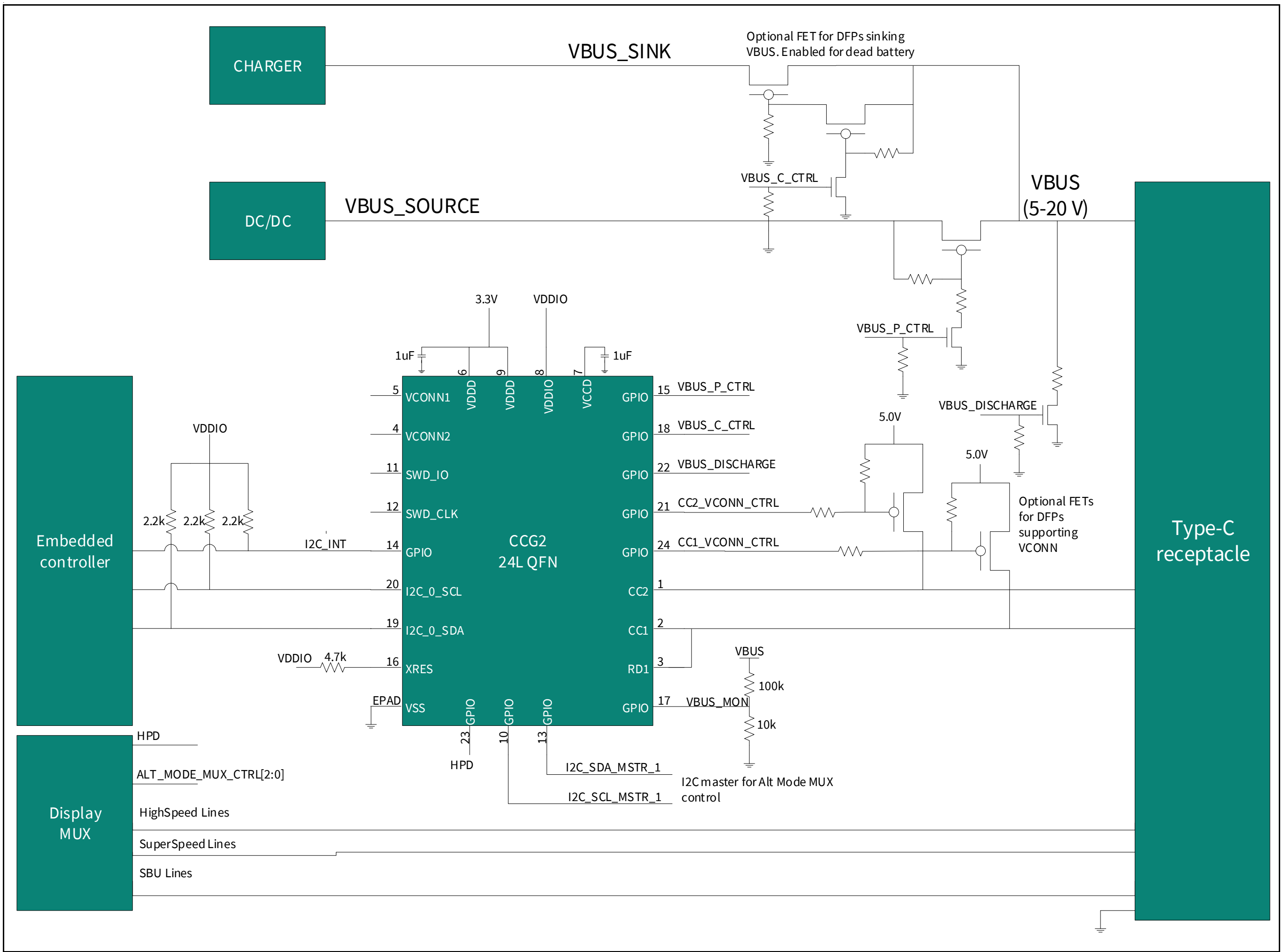


Figure 14 Dual role port (DRP) application (not recommended for new designs)

7.4 Downstream facing port applications

Figure 15 shows a CCG2 receptacle-based Power Adapter application in which the CCG2 device is used as a DFP. CCG2 integrates all termination resistors and uses GPIOs (VSEL_0 and VSEL_1) to indicate the negotiated power profile. The VBUS voltage on the Type-C port is monitored using internal ADC to detect undervoltage and overvoltage conditions on VBUS. To ensure quick discharge of VBUS when the power adapter cable is detached, a discharge path is also provided.

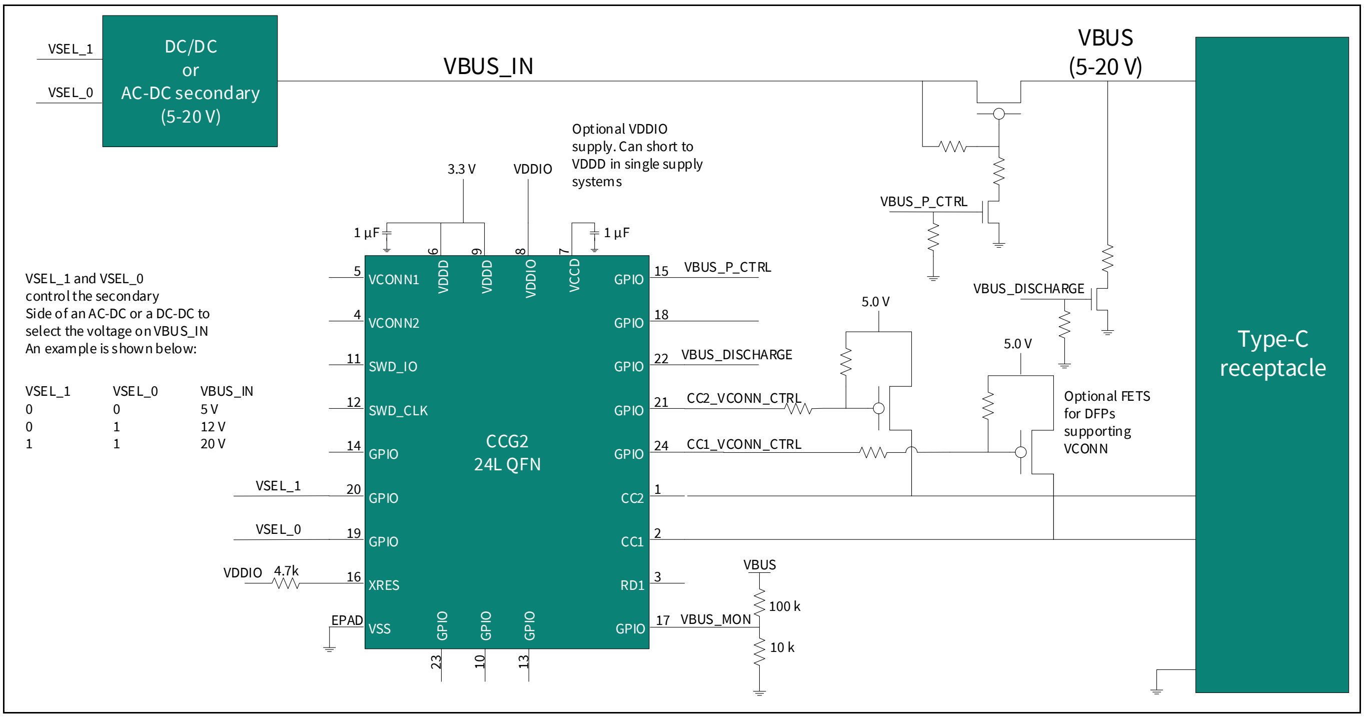


Figure 15 Downstream facing port (DFP) application

CCG2 is not recommended for new designs of Type-C to video dongles. CCG3 offers a much more integrated solution for this application and also supports PD3.0. Refer the **CCG3 datasheet** for more details. This section is just maintained for legacy purposes only.

8 Electrical specifications

8.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1]

Parameter	Description	Min	Typ	Max	Unit	Details/conditions
V_{DDD_MAX}	Digital supply relative to V_{SS}	–0.5	–	6	V	Absolute max
V_{CONN1_MAX}	Max supply voltage relative to V_{SS}	–	–	6		
V_{CONN2_MAX}	Max supply voltage relative to V_{SS}	–	–	6		
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	6		
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDIO} + 0.5		
V_{CC_ABS}	Absolute max voltage for CC1 and CC2 pins	–	–	6		
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5		Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model (ESD_HBM)	2200	–	–	V	–
ESD_CDM	ESD charged device model	500	–	–		
LU	Pin current for latch-up	–200	–	200	mA	
ESD_IEC_CON	ESD IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VCONN1, and VCONN2 pins
ESD_IEC_AIR	ESD IEC61000-4-2	15000	–	–		Air discharge for pins CC1, CC2, VCONN1, and VCONN2

Note

1. Usage of the absolute maximum conditions listed in **Table 2** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

8.2 Device level specifications

All specifications are valid for –40°C ≤ TA ≤ 85°C and TJ ≤ 100°C, except where noted. Specifications are valid for 3.0 V to 5.5 V, except where noted.

Table 3 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	UFP applications
SID.PWR#1_A	V_{DDD}		3.0	–	5.5		DFP/DRP applications
SID.PWR#23	V_{CONN1}		4.0	–	5.5		–
SID.PWR#23_A	V_{CONN2}		4.0	–	5.5		
SID.PWR#13	V_{DDIO}	GPIO power supply	1.71	–	5.5		
SID.PWR#24	V_{CCD}	Output voltage (for core logic)	–	1.8	–		
SID.PWR#15	C_{EFC}	External regulator voltage bypass on V_{CCD}	1	1.3	1.6	µF	X5R ceramic or better
SID.PWR#16	C_{EXC}	Power supply decoupling capacitor on V_{DDD}	–	1	–		
SID.PWR#25		Power supply decoupling capacitor on V_{CONN1} and V_{CONN2}	–	0.1	–		
Active mode, V_{DDD} = 2.7 V to 5.5 V. Typical values measured at V_{DD} = 3.3 V							
SID.PWR#12	I_{DD12}	Supply current	–	7.5	–	mA	V_{CONN1} or V_{CONN2} = 5 V, T_A = 25°C, CC I/O IN Transmit or Receive, R_A disconnected, no I/O sourcing current, CPU at 12 MHz.
Sleep mode, V_{DDD} = 2.7 V to 5.5 V							
SID25A	I_{DD20A}	I^2C wakeup. WDT ON. IMO at 48 MHz.	–	2.0	3.0	mA	V_{DDD} = 3.3 V, T_A = 25°C, all blocks except CPU are ON, CC I/O ON, no I/O sourcing current.
Deep Sleep mode, V_{DDD} = 2.7 V to 3.6 V (regulator on)							
SID_DS_RA	$I_{DD\_DS\_RA}$	V_{CONN1} = 5.0, R_A termination disabled	–	100	–	µA	V_{CONN1}, V_{CONN2} = 5 V, T_A = 25°C. R_A termination disabled on V_{CONN1} and V_{CONN2}, see SID.PD.7. VCONN leaker circuits turned off during deep sleep.
SID34	I_{DD29}	V_{DDD} = 2.7 to 3.6 V. I^2C wakeup and WDT ON	–	50	–		R_A switch disabled on V_{CONN1} and V_{CONN2}. V_{DDD} = 3.3 V, T_A = 25 °C
SID_DS	I_{DD_DS}	V_{DDD} = 2.7 to 3.6 V. CC wakeup ON	–	2.5	–		Power source = V_{DDD}, Type-C not attached, CC enabled for wakeup, R_P disabled.

Table 3 **DC specifications** *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
XRES current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	1	10	µA	–

Table 4 **AC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#4	F_{CPU}	CPU frequency	DC	–	48	MHz	3.0 V ≤ V_{DDD} ≤ 5.5 V
SID.PWR#20	T_{SLEEP}	Wakeup from Sleep mode	–	0	–	µs	Guaranteed by characterization
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	24-MHz IMO; Guaranteed by characterization.
SID.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	Guaranteed by characterization
SYS.FES#1	T_{PWR_RDY}	Power-up to “Ready to accept I2C / CC command”	–	5	25	ms	Guaranteed by characterization

8.2.1 I/O

Table 5 **I/O DC specifications**

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#37	V_{IH}[2]	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	V_{IH}[2]	LVTTL input, V_{DDIO} < 2.7 V	0.7 × V_{DDIO}	–	–	V	–
SID.GIO#40	V_{IL}	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	V_{IH}[2]	LVTTL input, V_{DDIO} ≥ 2.7 V	2.0	–	–	V	–
SID.GIO#42	V_{IL}	LVTTL input, V_{DDIO} ≥ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = 4 mA at 3 V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = 1 mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8 V V_{DDIO}
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 8 mA at 3 V V_{DDIO}
SID.GIO#5	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#6	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	kΩ	–
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{DDIO} = 3.0 V. Guaranteed by characterization.

Note

2. V_{IH} must not exceed V_{DDIO} + 0.2 V.

Table 5 I/O DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GIO#17	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.GIO#43	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DDIO} \geq 2.7$ V Guaranteed by characterization.
SID.GPIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DDIO}$	–	–	mV	Guaranteed by characterization.
SID69	I_{DIODE}	Current through protection diode to V_{DDIO}/Vss	–	–	100	µA	Guaranteed by characterization.
SID.GIO#45	I_{TOT_GPIO}	Maximum total source or sink chip current	–	–	200	mA	Guaranteed by characterization.

Table 6 I/O AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID70	T_{RISEF}	Rise time	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF

8.2.2 XRES

Table 7 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	$0.7 \times V_{DDIO}$	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	$0.3 \times V_{DDIO}$	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	Guaranteed by characterization
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	–	$0.05 \times V_{DDIO}$	mV	Guaranteed by characterization

8.3 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

8.3.1 Pulse width modulation (PWM) for GPIO pins

Table 8 PWM AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	F_C	–	MHz	F_C max = CLK_SYS Maximum = 48 MHz
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	–	$2/F_C$	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	–	$2/F_C$	–		Minimum possible width of overflow, underflow, and CC (counter equals compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	–	$1/F_C$	–		Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	–	$1/F_C$	–		Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	–	$1/F_C$	–		Minimum pulse width between quadrature-phase inputs

8.3.2 I^2C

Table 9 Fixed I^2C DC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	I_{I2C1}	Block current consumption at 100 kbps	–	–	60	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kbps	–	–	185		–
SID151	I_{I2C3}	Block current consumption at 1 Mbps	–	–	390		–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	–	1.4		–

Table 10 Fixed I^2C AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

Table 11 Fixed UART DC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 Kbps	–	–	125	µA	Guaranteed by characterization
SID161	I_{UART2}	Block current consumption at 1000 Kbps	–	–	312		

Table 12 Fixed UART AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	Guaranteed by characterization

Table 13 Fixed SPI DC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	I_{SPI1}	Block current consumption at 1 Mbps	–	–	360	µA	Guaranteed by characterization
SID164	I_{SPI2}	Block current consumption at 4 Mbps	–	–	560		
SID165	I_{SPI3}	Block current consumption at 8 Mbps	–	–	600		

Table 14 Fixed SPI AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	F_{SPI}	SPI Operating frequency (Master; 6X oversampling)	–	–	8	MHz	Guaranteed by characterization

Table 15 Fixed SPI master mode AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	T_{DMO}	MOSI Valid after SClock driving edge	–	–	15	ns	Guaranteed by characterization
SID168	T_{DSI}	MISO Valid before SClock capturing edge	20	–	–		Full clock, late MISO sampling. Guaranteed by characterization
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–		Referred to Slave capturing edge. Guaranteed by characterization

Table 16 Fixed SPI slave mode AC specifications

(Guaranteed by characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	T_{DMI}	MOSI Valid before Sclock Capturing edge	40	–	–	ns	Guaranteed by characterization
SID171	T_{DSO}	MISO Valid after Sclock driving edge	–	–	42 + 3 * T_{CPU}		TCPU = 1/FCPU. Guaranteed by characterization.
SID171A	T_{DSO_EXT}	MISO Valid after Sclock driving edge in Ext Clk mode	–	–	48		Guaranteed by characterization
SID172	T_{HSO}	Previous MISO data hold time	0	–	–		
SID172A	$T_{SSELSCK}$	SSEL Valid to first SCK Valid edge	100	–	–		

8.4 Memory

Table 17 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.MEM#4	$T_{ROWWRITE}$[3]	Row (block) write time (erase and program)	–	–	20	ms	Row (block) = 128 bytes
SID.MEM#3	$T_{ROWERASE}$[3]	Row erase time	–	–	13		–
SID.MEM#8	$T_{ROWPROGRAM}$[3]	Row program time after erase	–	–	7		
SID178	$T_{BULKERASE}$[3]	Bulk erase time (32 KB)	–	–	35		
SID180	$T_{DEVPROG}$[3]	Total device program time	–	–	7.5	seconds	Guaranteed by characterization
SID181	F_{END}	Flash endurance	100 K	–	–	cycles	
SID182	F_{RET1}	Flash retention. $T_A \leq 55$ °C, 100 K P/E cycles	20	–	–	years	
SID182A	F_{RET2}	Flash retention. $T_A \leq 85$ °C, 10 K P/E cycles	10	–	–		

Note

3. It can take as much as 20 milliseconds to write to flash. During this time the device should not be reset, or flash operations will be interrupted and cannot be relied on to have completed. Reset sources include the XRES pin, software resets, CPU lockup states and privilege violations, improper power supply levels, and watchdogs. Make certain that these are not inadvertently activated.

8.5 System resources

8.5.1 Power-on-reset (POR) with brownout

Table 18 Imprecise POR (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.75	–	1.4		

Table 19 Precise POR

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID190	$V_{FALLPPOR}$	BOD trip voltage in Active and Sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.1	–	1.5		

8.5.2 SWD interface

Table 20 SWD interface specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	$F_{SWDCLK1}$	3.3 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	$F_{SWDCLK2}$	1.8 V ≤ V_{DDIO} ≤ 3.3 V	–	–	7		
SID.SWD#3	T_{SWDI_SETUP}	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_{SWDI_HOLD}	T = 1/f SWDCLK	0.25*T	–	–		
SID.SWD#5	T_{SWDO_VALID}	T = 1/f SWDCLK	–	–	0.5 * T		
SID.SWD#6	T_{SWDO_HOLD}	T = 1/f SWDCLK	1	–	–		

8.5.3 Internal main oscillator

Table 21 IMO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID218	I_{IMO}	IMO operating current at 48 MHz	–	–	1000	µA	–

Table 22 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 24, 36, and 48 MHz (trimmed)	–	–	±2	%	–
SID226	$T_{STARTIMO}$	IMO startup time	–	–	7	µs	Guaranteed by characterization
SID229	$T_{JITRMSIMO}$	RMS jitter at 48 MHz	–	145	–	ps	
–	F_{IMO}	IMO frequency	24	–	48	MHz	–

8.5.4 Internal low-speed oscillator

Table 23 ILO DC specifications

(Guaranteed by design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID231	I_{ILO}	ILO operating current at 32 kHz	–	0.3	1.05	µA	Guaranteed by characterization
SID233	$I_{ILOLEAK}$	ILO leakage current	–	2	15	nA	Guaranteed by design

Table 24 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID234	$T_{STARTILO}$	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	$T_{ILODUTY}$	ILO duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	ILO frequency	20	40	80	kHz	–

8.5.5 Power down

Table 25 PD DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.1	Rp_std	DFP CC termination for default USB Power	64	80	96	µA	–
SID.PD.2	Rp_1.5A	DFP CC termination for 1.5A power	166	180	194		
SID.PD.3	Rp_3.0A	DFP CC termination for 3.0A power	304	330	356		
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	
SID.PD.5	Rd_DB	UFP Dead Battery CC termination on RD1 and CC2	4.08	5.1	6.12		All supplies forced to 0 V and 0.6 V applied at RD1 or CC2
SID.PD.6	R_A	Power cable termination	0.8	1.0	1.2		All supplies forced to 0 V and 0.2 V applied at V_{CONN1} or V_{CONN2}
SID.PD.7	Ra_OFF	Power cable termination - Disabled	0.4	0.75	–	MΩ	2.7 V applied at V_{CONN1} or V_{CONN2} with R_A disabled
SID.PD.8	Rleak_1	V_{CONN} leaker for 0.1-µF load	–	–	216	kΩ	Managed Active Cable (MAC) discharge
SID.PD.9	Rleak_2	V_{CONN} leaker for 0.5-µF load	–	–	41.2		
SID.PD.10	Rleak_3	V_{CONN} leaker for 1.0-µF load	–	–	19.6		
SID.PD.11	Rleak_4	V_{CONN} leaker for 2.0-µF load	–	–	9.8		
SID.PD.12	Rleak_5	V_{CONN} leaker for 5.0-µF load	–	–	4.1		
SID.PD.13	Rleak_6	V_{CONN} leaker for 10-µF load	–	–	2.0		
SID.PD.14	Ileak	Leaker on V_{CONN1} and V_{CONN2} for discharge upon cable detach	150	–	–	µA	–

8.5.6 Analog to digital converter

Table 26 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	bits	Guaranteed by characterization
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5		
SID.ADC.4	Gain error	Gain error	–1	–	1		

Table 27 ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ADC.5	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	Guaranteed by characterization

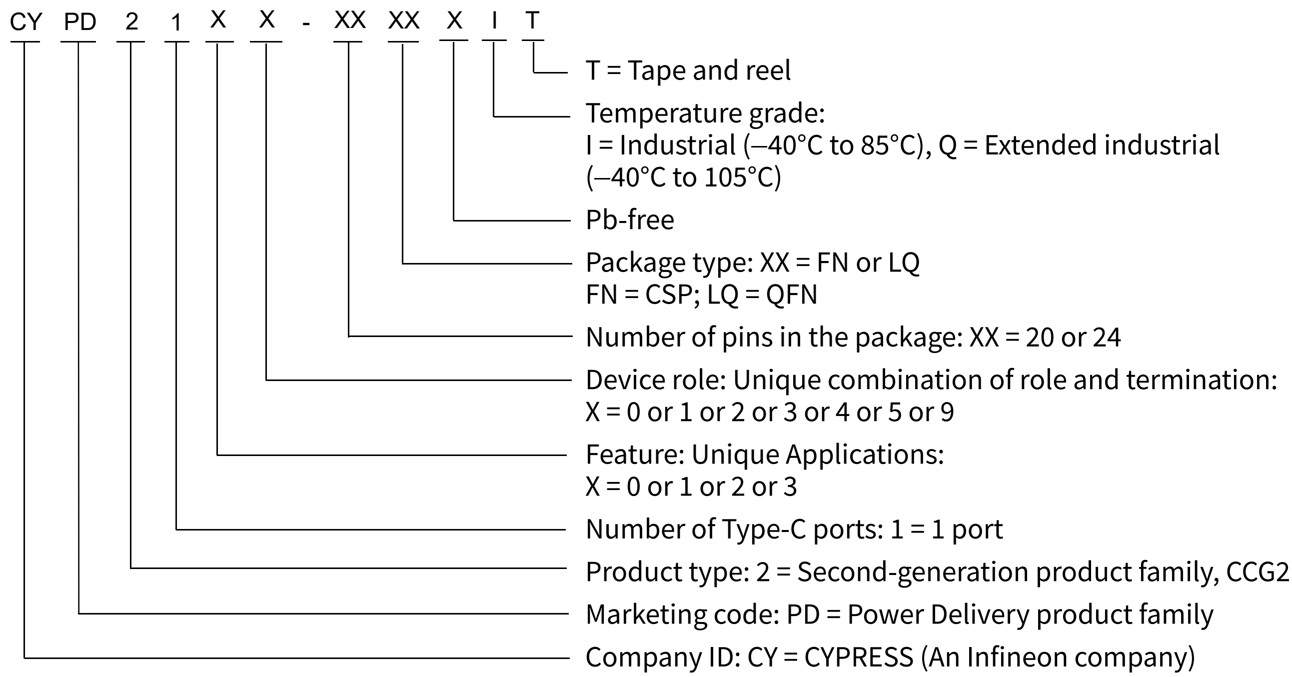
9 Ordering information

The EZ-PD™ CCG2 part numbers and features are listed in **Table 28**.

Table 28 EZ-PD CCG2 ordering Information

<table>
<tr><th>Product[4]</th><th>Application</th><th>Type-C ports</th><th>Termination resistor</th><th>Role</th><th>Package</th></tr>
<tr><td>CYPD2104-20FNXIT</td><td>Accessory</td><td rowspan="5">1</td><td>R_P, R_D, R_{D-DB}</td><td>I^{2}C bootloader only</td><td>20-ball CSP</td></tr>
<tr><td>CYPD2105-20FNXIT</td><td>Active Cable</td><td>R_A</td><td>EMCA CC bootloader with application firmware</td><td>20-ball CSP</td></tr>
<tr><td>CYPD2122-24LQXI</td><td>Notebook</td><td>R_P, R_D, R_{D-DB}</td><td rowspan="2">I^{2}C bootloader only</td><td>24L QFN</td></tr>
<tr><td>CYPD2122-24LQXIT</td><td>Notebook</td><td>R_P, R_D, R_{D-DB}</td><td>24L QFN</td></tr>
<tr><td>CYPD2134-24LQXQT</td><td>DFP</td><td>R_P</td><td>DFP CC bootloader only</td><td>24L QFN</td></tr>
</table>

9.1 Ordering code definitions



10 Packaging

Table 29 Package characteristics

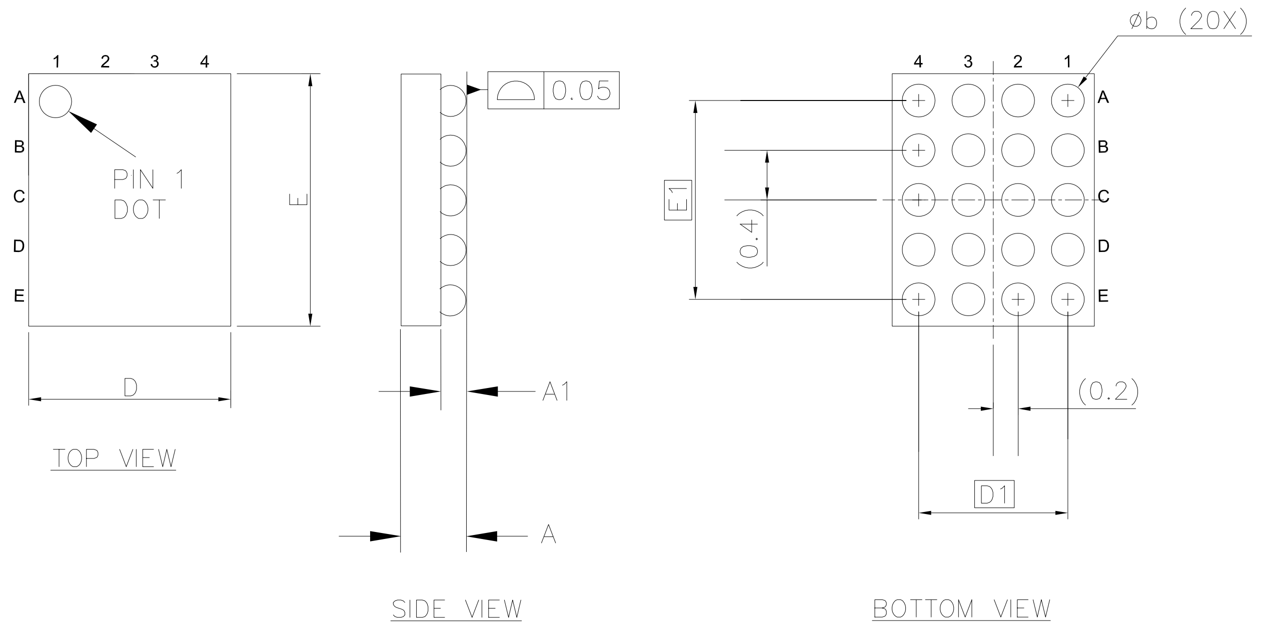
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
		Extended industrial			105	
T_J	Operating junction temperature	Industrial	–40	–	100	
		Extended industrial			125	
T_{JA}	Package θ_{JA} (20-ball WLCSP)	–	–	66	–	°C/W
T_{JC}	Package θ_{JC} (20-ball WLCSP)			0.7		
T_{JA}	Package θ_{JA} (24L QFN)			22		
T_{JC}	Package θ_{JC} (24L QFN)			29		

Table 30 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
20-ball WLCSP	260 °C	30 seconds
24L QFN		

Table 31 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
20-ball WLCSP	MSL 1
24L QFN	MSL 3



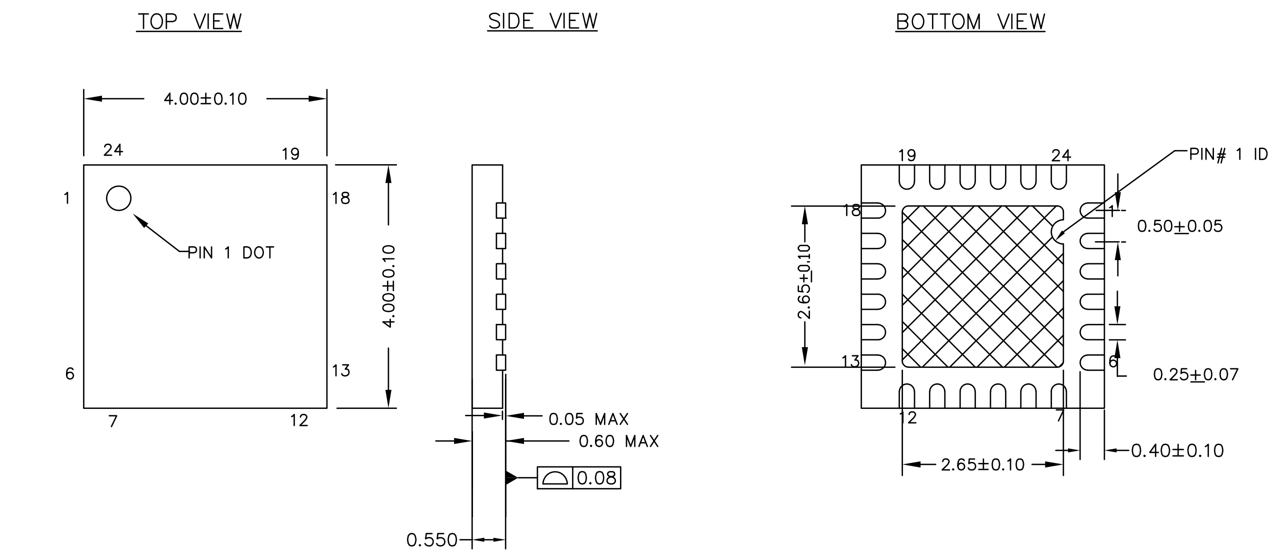
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.55
A1	0.18	0.21	0.24
D	1.605	1.63	1.655
E	2.005	2.03	2.055
D1	1.2 BSC		
E1	1.6 BSC		
n	20		
Øb	0.23	0.26	0.29

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18

001-95010 *B

Figure 16 20-ball WLCSP (1.63 × 2.03 × 0.55 mm) FN20B (SG-XFWLB-20) package outline



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *H

Figure 17 24L QFN (4 × 4 × 0.55 mm), LQ24A, 2.65 × 2.65 E-Pad (Sawn) (PG-VQFN-24) package outline

11 Acronyms

Table 32 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
ARM®	advanced RISC machine, a CPU architecture
CC	configuration channel
CCG2	Cable Controller Generation 2
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MAC	managed active cable
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery

Table 32 Acronyms used in this document *(continued)*

Acronym	Description
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on-reset
PRES	precise power-on reset
PSoC™	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USBIO	USB input/output, CCG2 pins used to connect to a USB port
XRES	external reset I/O pin

12 Document conventions

12.1 Units of measure

Table 33 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*G	2015-06-15	Changed datasheet status from Preliminary to Final. Updated Logic Block Diagram. Changed number of GPIOs to 10 and added a note about the number of GPIOs varying depending on the package. Updated Power and Digital Peripherals section. Updated Application diagrams. Added SID.PWR#1_A parameter. Added CYPD2122-20FNXIT part in Ordering Information. Removed Errata.
*H	2015-10-23	Updated **Figure 1** and **Figure 4**. Added VCC_ABS spec and updated the SID.ADC.4 parameter. Added "Guaranteed by characterization" note for the following specs: SID.GIO#16, SID.GIO#17, SID.XRES#3, SID 160 to SID 172A, SID 2226, SID 229, SID.ADC.1 to SID.ADC.5.
*I	2015-12-04	Updated **Application diagrams**: Added Figure 12. Added Figure 13. Added Figure 14. Updated **Ordering information**. Added part numbers CYPD2119-24LQXIT, CYPD2120-24LQXIT, CYPD2121-24LQXIT, CYPD2125-24LQXIT.
*J	2016-03-28	Updated temperature ranges in **Features**. Updated **Table 28**. Updated **Ordering information**.
*K	2016-06-13	Added **Available firmware and software tools**. Updated **Figure 11**: Per the USB PD3.0 spec, SOP" implementation is no longer valid for passive cables. Updated **Figure 13**, **Figure 14**, and **Figure 15**. Added descriptive notes for the application diagrams. Added References and Links to Applications Collaterals. Updated **Ordering information**. Updated Cypress logo and copyright information
*L	2016-08-02	Added CYPD2122-24LQXI part number in **Ordering information**.
*M	2018-07-11	Added **Figure 10** and **Figure 12**. Updated the title of **Figure 9** and **Figure 11**. Added "Note: Application diagram in Figure 8 requires external diodes to operate in the extended VCONN voltage range of 2.7V to 5.5V" in **Application diagrams**. Updated **Figure 16** (Spec 001-95010 from *A to *B). Updated **Figure 17** (Spec 001-13937 from *F to *G). Added compliance to USB Specification. Updated Cypress Logo and Copyright year.
*N	2020-12-04	Updated **Figure 6** in **Power** section. Added **CCG2 Programming and Bootloading** section. Updated descriptions before all application diagrams in **Application diagrams** section. Added column "Default FW" in **Table 28** in **Ordering information** section. Updated **Figure 17** in **Packaging** section.

Document revision	Date	Description of changes
*O	2024-05-10	Updated **Table 28** in Ordering information: Removed part numbers – CYPD2103-14LHXIT, CYPD2103-20FNXIT, CYPD2125-24LQXIT, CYPD2121-24LQXIT, CYPD2120-24LQXIT, CYPD2119-24LQXIT, and CYPD2122-20FNXIT. Removed information related to 14-DFN package in the document. Removed sections – C-HDMI Dongle Application, C-DisplayPort (DP) Dongle Application, and Dock/monitor Application. Removed Figure 9. Updated to Infineon package naming convention: 24-pin QFN to 24L QFN. Updated package diagram (**Figure 16** and **Figure 17**) titles with Infineon package code. Migrated to Infineon template.

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